SPECIFICATION

TITLE OF INVENTION

STACKED CHIP PACKAGE WITH HEAT TRANSFER WIRE

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a conventional stacked chip package.

FIG. 2 shows the thermal characteristics of the stacked chip package of FIG. 1 by a simulation.

FIG. 3 is a plan view of a stacked chip package according to a first embodiment of the present invention.

FIG. 4 is a cross-sectional view of the stacked chip package taken along 4-4 of FIG. 3.

FIG. 5 is a cross-sectional view of the stacked chip package taken along 5-5 of FIG. 3.

FIG. 6 is a plan view of a stacked chip package according to a second embodiment of the present invention.

FIG. 7 is a plan view of a stacked chip package according to a third embodiment of the present invention.

FIG. 8 is a cross-sectional view of a stacked chip package according to a fourth embodiment of the present invention.

* REFERENCE NUMERALS *

110, 210, 310, 410: board

111, 211, 311, 411: board pad

111a, 211a, 311a, 411a: dummy board pad

115, 415: solder ball pad

115a, 415a: dummy solder ball pad

116, 416: via hole

116a, 416a: dummy via hole

121, 221, 321, 421: first chip

223a, 323a: dummy bonding pad

122, 222, 322, 422: second chip

132, 232, 332, 432: first bonding wire

134, 434: second bonding wire

136, 236, 336, 436, 438: heat transfer wire

140, 440: adhesive layer

150, 450: resin encapsulant

160, 460: solder ball

160a, 460a: dummy solder ball pad

200, 300, 400, 500: stacked chip package

DETAILED DESCRIPTION OF THE INVENTION

OBJECT OF THE INVENTION

FIELD OF THE INVENTION AND RELATED ART

The present invention relates to a semiconductor package and, more particularly, to a stacked chip package having a heat transfer wire to dissipate heat trapped between chips.

A conventional semiconductor wafer may have technical limitations in enhancing the density of chips for purposes of making them highly integrated. Therefore, three-dimensional semiconductor packaging technologies have been developed and are being used. In general, package stacks made by stacking a plurality of packages, and stacked chip packages made by stacking a plurality of chips, are broadly known.

The former is possible to achieve high density of integration by using package stacks. However, the thickness of the individual packages may increase the thickness of the package stacks.

Compared with package stacks, the latter is possible not only to achieve a high density of integration but also to minimize the thickness by using stacked chip packages.

Referring to FIG. 1, the conventional structure of the stacked chip package (100) will be explained. As shown in FIG. 1, two chips (21, 22) are stacked on a substrate (10). The two stacked chips (21, 22) are connected to the substrate (10) electrically by bonding wires (32, 34). The chips (21, 22) and the bonding wires (32, 34) are sealed by a resin encapsulant (50). On the rear side of the substrate (10), solder balls (60) are formed and connected to the chips (21, 22). The lower chip (21) is hereinafter referred to as a first chip and the upper chip (22) is hereinafter referred to as a second chip.

However, there is a thermal dissipation problem in the conventional stacked chip package (100) shown in FIG. 1. The technical problem in connection with heat dissipation is described in FIG. 2. As shown in FIG. 2, heat is generated by the first chip (21) during operation of the first chip (21). The generated heat is transferred to an adhesive layer (40) through the active surface of the first chip (21). But the adhesive layer (40) is non-conductive and has a relatively low heat transfer characteristics. Further the second chip (22) is stacked on the adhesive layer (40). Therefore, the heat generated by the first chip (21) is trapped between the first and second chips (21, 22).

If the heat trapped in an adhesive layer (40) cannot be dissipated, it can result in heating of the first and second chips (21, 22), especially heating of the first chip (21). Therefore, the performance of the stacked chip package (100) will deteriorate, if the technical problem of the heat trapped in the adhesive layer (40) cannot be solved.

TECHNICAL SUBJECT TO BE SOLVED

Therefore, the present invention is directed to provide a stacked chip package which may dissipate heat trapped between chips to the external.

CONSTITUTION OF THE INVENTION

In order to solve the above-mentioned problems, the present invention provides a stacked chip package having at least one heat transfer wire. The heat transfer wire is disposed between the stacked chips and at least one end of each transfer wire is connected to a dummy pad provided on the board. Therefore, the heat generated by the chips and trapped between the chips can be effectively dissipated.

In one embodiment, a stacked chip package comprises a board having board pads; a first chip having bonding pads; a first bonding wire connecting the bonding pad of the first chip with the board; a second chip stacked on the first chip using a nonconductive adhesive layer and having bonding pads; a second bonding wire connecting the bonding pad of the second chip with the board; a resin encapsulant sealing the first and second chips and the first and second bonding wires; and solder balls formed at the rear side of the board and electrically connected with the first and second chips.

The stacked chip package further comprises at least one heat transfer wires disposed between the first and second chips. At least one end of each heat transfer wire is attached to the board.

The bonding pad of the first chip may be arranged along the opposite edges of the active surface of the first chip. The heat transfer wires may be formed parallel to the bonding pad arranging edge. The board may have bonding pads. The bonding pads may include at least one dummy board pad to be connected to the heat transfer wire.

Preferably, a plurality of solder balls may be provided on the rear side of the board, and electrically connected to the board pads and the dummy board pads. Preferably, at least one of the heat transfer wires may be used for connecting means to ground.

Dummy bonding pads may be arranged along opposite edges perpendicular to the bonding pad arranging edge of the first chip. The heat transfer wire may connect the dummy bonding pad and the corresponding dummy board pad. Alternatively, the dummy bonding pads may be arranged at the center portion of the active surface of the first chip. Or the dummy bonding pads may be in a zigzag fashion arranged along the edges perpendicular to

the bonding pad arranging edges. The heat transfer wire may connect the dummy bonding pad at one edge and the dummy board pad at the opposite edge.

The bonding pad of the second chip may be arranged along the opposite edge. A second heat transfer wire may be formed over the second chip.

The stacked chip package according to a first embodiment of the present invention is illustrated in FIG. 3., FIG. 4, and FIG. 5.

FIG. 3 is a plan view of the stacked chip package having at least one heat-transfer wire (136). In FIG. 3, a second chip (122) is not fully depicted, in order to show the heat-transfer wires (136) disposed on the first chip (121).

According to the first embodiment of the present invention, first and second chips (121, 122) are stacked on a board (110) three-dimensionally. The first and second chips (121, 122) are sealed by a resin encapsulant (150). External connection terminals (160) such as solder balls are formed on the rear side of the board (110). In order to dissipate the heat generated by the first and second chips (121, 122) which is trapped in the adhesive layer (140), the heat-transfer wires (136) are disposed between the first chip (121) and the second chip (122). One end of each heat-transfer wire (136) is attached to the board (110).

Preferably, the board (110) is a printed circuit board (PCB). The board (110) is composed of a board body (112), and a plurality of metal wiring patterns (114) formed on the board body (112). The metal wiring patterns (114) comprise upper wiring patterns including board pads (111), and lower wiring patterns having solder ball pads (115). The board pads (111) are connected to the chips (121, 122) by the bonding wires (132, 134) and solder balls (160) are formed on the solder ball pads (115). Preferably, the metal wiring patterns (114) may be manufactured by patterning laminated copper foils on the board body (112). A solder resist layer (118) is formed on substantially the entire area of the board (110) except for the solder ball pads (115) and the board pads (111). Preferably, the solder ball pads (115) are electrically connected to the board pads (111) by via holes (116) formed thorough the board body (112).

Dummy board pads (111a) are provided on the board body (112) to be bonded with heat transfer wires 136. Preferably, the dummy board pads (111a) are connected to the dummy solder ball pads (115a) by dummy via holes (116a). The dummy board pads (111a), the dummy via holes (116a), and the dummy solder ball pads (115a) are used for heat transfer, and not for electrical connection between the chips (121,122) and outer terminals. However, the dummy board pads (111a), the dummy via holes (116a) and the dummy solder ball pads (115a) may be used as the connecting means to ground.

Although a printed circuit board (PCB) is disclosed as the board (110) in the first embodiment of the present invention, for example, a lead frame, a tape circuit board or a ceramic board can also be used as the board (110).

According to a first embodiment of the present invention, a plurality of bonding pads (123) are formed along opposite edges of the first chip (121). The first chip (121) has a non-conductive adhesive layer (127) on the back surface. Bonding bumps (125) are formed on the bonding pads (123). The first chip (121) is attached to the board (110) by the non-conductive adhesive layer (127).

Although this embodiment shows the first chip (121) has the non-conductive adhesive layer (127) formed on the back surface, the first chip may not have a non-conductive adhesive layer. In this case, an adhesive may be applied to a board and a first chip may be attached to the board.

The bonding pad (125) is electrically connected to the board pad (111) by the first bonding wire (132). In order to reduce the height of the bonding wire loop, each first bonding wire (132) is connected to the board pad (111) by ball bonding, and connected to the bonding pad (123) by stitch bonding.

The dummy bonding pad (123) is connected to the dummy board pad (111a) by the heat-transfer wire (136). Preferably, the heat transfer wires (136) are formed by using wire bonding methods. One end of each heat transfer wire (136) is connected to a dummy board pad (111a) by ball bonding, and the other end of the heat transfer wire (136) is connected to another dummy board pad (111a) by stitch bonding. Although it is desirable for the heat transfer wires (136) to be separated from the first chip (121), there is no electric-short problem even if the heat transfer wires (136) are in contact with the first chip (121).

Preferably, a metal such as Au or Al having excellent heat conductivity is used to form the heat transfer wires (136).

The second chip (122) has bonding pads (124) arranged along the opposing edges of the active surface. A non-conductive layer (128) may be formed beneath the second chip (122), in order to prevent an electrical short between the second chip (122) and the first bonding wires (132). Each bonding pad (124) has bonding bump (126). The second chip (122) is attached to the active surface of the first chip (121) using a non-conductive adhesive (140). Although this embodiment shows the first and second chips (121, 122) are the same type semiconductors, the first and second chips (121, 122) may be different type semiconductors. In this case, the first and second chips (121, 122) may be stacked on the board (110) with the bonding pads (123, 124) corresponding to each other. To prevent the

interference of the heat transfer wires, the first and second chips (121, 122) may be stacked with the bonding pad being arranged in the same direction.

The bonding pads (124) of the second chip (122) are connected to the board pads (111) by second bonding wires (134). In order to reduce the height of the bonding wire loop, each first bonding wire (132) is connected to the board pad (111) by ball bonding, and connected to the bonding pad (123) by stitch bonding.

The first and second chips (121, 122), the first and second bonding wires (132, 134) and the heat transfer wires (136) are sealed by the resin encapsulant (150) to protect them from the external environment.

According to the first embodiment of the present invention, the external connection terminals (160) such as solder balls are formed on the rear side of the board (110). The solder balls (160) are electrically connected with the board pads (111) through the via holes (116). The solder balls (160) include dummy solder balls (160a). The dummy solder balls (160a) are formed on the dummy solder ball pads (115a). The dummy solder ball pads (115a) connected to the dummy board pads (111a) through the dummy via holes (116a).

The heat generated by operation of the stacked chip package (200) and trapped between the first and second chips (121, 122) can be transferred to the dummy board pads (111a), the dummy via holes (116a), the dummy solder ball pads (115a) and the dummy solder balls (160a) through the heat transfer wires (136) and dissipated to the external. The heat transfer wires (136) may provide a path for dissipating heat trapped between the first and second chips (121, 122) to the external.

Because the heat transfer wires (136) can be manufactured using conventional wire bonding method, there is no need for an additional process or apparatus for manufacturing the heat transfer mechanism. In addition, the thermal characteristics of the stacked chip package (200) can be calibrated by controlling the number or the size of the heat transfer wires (136).

Although the first embodiment shows the corresponding dummy board pads (111a) at each side of the first chip (121) are connected by the heat transfer wires 136, the dummy bonding pads (223a) are provided on substantially the center portion of the first chip (221) and dummy board pads (211a) are connected to dummy bonding pads (223a) by heat transfer wires (236).

In FIGs. 6 and 7, a second chip is not fully depicted, in order to show the heat transfer wires and dummy bonding pads.

As shown in FIG. 6, dummy bonding pads (223a) are arranged adjacent to the center portion of the first chip (221). The bonding pads (223) are provided along the edges of the

first chip (221) separated from the dummy bonding pads (223a). The dummy bonding pads (223a) are used for heat dissipation, not for electrical connection purposes. However, it is possible for the dummy bonding pads (223a) to be used for connection means to ground.

Each dummy bonding pad (223a) has dummy bonding bump (227a). One end of each heat transfer wire (236) is connected to a dummy bonding pad (223a) by stitch bonding, and the other end is connected to a dummy board pad (211a) formed on a board (210) similar to the board (110) of FIG. 3 by ball bonding.

Referring to FIG. 7, according to a third embodiment of the present invention, dummy bonding pads (323a) are provided on opposite edges of the first chip (321). Preferably, the dummy bonding pads (323a) are separated from the bonding pads (323). As with the first and second embodiments, the dummy bonding pads (323a) are used for heat dissipation, not for electrical connection purposes. However, it is possible for the dummy bonding pads (323a) to be used for connection to ground.

One end of each heat transfer wire (336) is connected to a dummy bonding pad (323a), preferably by stitch bonding, and the other end is connected to a dummy board pad (311a), preferably by ball bonding. For stable stitch bonding, dummy bonding bumps (327a) may be formed on the dummy bonding pad (323a) before the stitch bonding is performed to connect the heat transfer wire (336) with the dummy bonding pad (323a). The dummy bonding pads (232a) are positioned apart from the correspondingly connected dummy board pads (311a), in order to increase the area of the first chip (321) covered with the heat transfer wires (336).

Although the third embodiment shows the dummy bonding pad (323a) is arranged along the opposite edges of the first chip (321), the dummy bonding pad (323a) may be formed on the first chip (321) adjacent one edge of the first chip (321). The dummy board pad (311a) is formed on a board (310) adjacent to the edge of the first chip (321) opposite the one edge.

Referring to FIG. 8, according to the fourth embodiment of the present invention, upper heat transfer wires (438) are provided on the second chip (422) in order to enhance the heat dissipation of the second chip (422). The upper heat transfer wire 438 is hereinafter referred to as a second heat transfer wire. The lower heat transfer wire 436 is hereinafter referred to as a first heat transfer wire.

A stacked chip package (500) is the same with the stacked chip package (200) of the first embodiment, except that the second heat transfer wire (438) is connected to the dummy board pad (411a), to which the first heat transfer wire (436) is connected. Heat generated

between the first and second chips (421, 422) is dissipated through the first heat transfer wires (436). Heat generated from the second chip (422) is dissipated through the second heat transfer wire (438). Therefore, the heat generated by the stacked chip package (500) can be more easily dissipated by both the first heat transfer wires (436) and the second heat transfer wires (438).

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. For example, the second heat transfer wire may be also applied to the second and third embodiments. Further, although the stacked chip package made by stacking only two chips is described in the embodiments of the present invention, it should be apparent to a person skilled in the art that the present invention can be applied to the stacked chip package made by stacking more than two chips.

EFFECT OF THE INVENTION

According to the present invention, the heat transfer wires disposed between stacked chips can transfer the heat out of the stacked chip package, and the heat transfer wires may not increase the thickness of the stacked chip package.

Further, the heat transfer wires can be easily manufactured by the wire bonding method, so that there is no need for a special process or apparatus for manufacturing the heat dissipation means. Therefore, a cost-saving heat dissipation means is provided in the present invention.

In addition, the thermal characteristics of the stacked chip package can be calibrated by controlling the number or the size of the heat transfer wires.